



# DF329

## 3-Phase Brushless DC Motor Controller

### *Data Sheet*

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# DF329

## 3-Phase Brushless DC Motor Controller

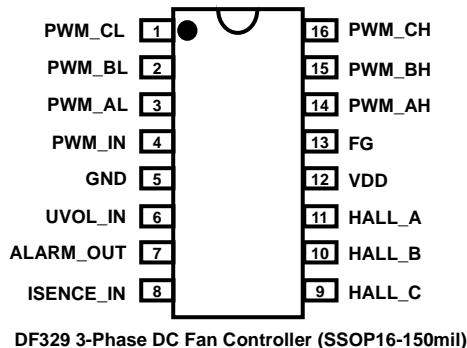
### Revision History:

Revision	Date	Description
0.00	2018/10/29	Preliminary version
0.01	2019/01/25	Amend $f_{IHRC}$ in Section 3.1
0.02	2019/03/06	Amend $V_{POR}$ in Section 3.1

## 1. Key Features

- ◆ Support 3-Phase brushless DC motor with hall IC interface
- ◆ Support PWM control input or voltage control input
- ◆ Support FG/RD/ALM/RALM/RXX/RRXX output
- ◆ Support alarm output
- ◆ Support reverse brake control
- ◆ Support software hall degree forward and backward
- ◆ Support close loop control and open loop control
- ◆ Support current limitation and current protection
- ◆ Support under voltage over low protection
- ◆ Support soft-start
- ◆ Support lock-protect and auto-restart
- ◆ Built-in internal RC clock oscillator
- ◆ 5V operating voltage

## 2. DF329 Pin Assignment and Description



DF329 3-Phase DC Fan Controller (SSOP16-150mil)

Pin No.	Pin Name	I/O	Description
1	PWM_CL	Output	C output signal to control the low side of motor driver
2	PWM_BL	Output	B output signal to control the low side of motor driver
3	PWM_AL	Output	A output signal to control the low side of motor driver
4	PWM_IN	Input	PWM control input
5	GND	-	Ground
6	UVOL_IN	Input	Analog input to sense motor voltage
7	ALARM_OUT	Output	Digital output to motor alarm
8	ISENSE_IN	Input	Analog input to sense motor current
9	HALL_C	Input	Digital input to sense motor position C
10	HALL_B	Input	Digital input to sense motor position B
11	HALL_A	Input	Digital input to sense motor position A
12	VDD	-	Positive power
13	FG	Output	Rotation speed detection
14	PWM_AH	Output	A output signal to control the high side of motor driver
15	PWM_BH	Output	B output signal to control the high side of motor driver
16	PWM_CH	Output	C output signal to control the high side of motor driver

### 3. DC Characteristics

#### 3.1. AC/DC Device Characteristics

<b>Symbol</b>	<b>Description</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>	<b>Unit</b>	<b>Conditions (Ta=25°C)</b>
$V_{DD}$	Operating Voltage	3.5 4.75	5.0 5.0	5.5 5.5	V	-40 °C < Ta < 85 °C -40 °C < Ta < 105 °C
$V_{FSV}$	Forbidden $V_{DD}$ Startup voltage Range*	0.7		1.6	V	
$V_{PDRV}$	$V_{DD}$ power down release voltage			0.7	V	
$T_{POR}$	$V_{DD}$ power on time ( $V_{DD}$ from 0V to 5V)			50	ms	
$T_{FSV}$	$V_{DD}$ power on time during $V_{FSV}$ range			10	ms	
$V_{IL}$	Input low voltage for IO lines	0		0.2 $V_{DD}$	V	
$V_{IH}$	Input high voltage for IO lines	0.8 $V_{DD}$		$V_{DD}$	V	
$I_{OP}$	Operating Current		10		mA	
$I_{OL}$	IO lines sink current	7	10	13	mA	$V_{DD}=5.0V$ , $V_{OL}=0.5V$
$I_{OH}$	IO lines drive current	-5	-7	-9	mA	$V_{DD}=5.0V$ , $V_{OH}=4.5V$
$R_{PH}$	Pull-high Resistance		62 100		KΩ	$V_{DD}=5.0V$ $V_{DD}=3.3V$
$V_{LVR}$	Low Voltage Reset*	3.31	3.60	3.89	V	
$V_{POR}$	Power-On Reset Voltage	1.8	2	2.3	V	Ta=25°C
$f_{IHRC}$	Frequency of IHRC after calibration *	15.68*	16*	16.32*	MHz	25°C, $V_{DD}=3.5V\sim 5.5V$
		15.36*	16*	16.64*		$V_{DD}=3.5V\sim 5.5V$ , 0°C < Ta < 85°C*
		15.2*	16*	16.8*		$V_{DD}=4.75V\sim 5.5V$ , 0°C < Ta < 105°C*
		14.72*	16*	17.28*		$V_{DD}=3.5V\sim 5.5V$ -20°C < Ta < 85°C
		14.56*	16*	17.44*		$V_{DD}=4.75V\sim 5.5V$ -20°C < Ta < 105°C*
		14.08*	16*	17.92*		$V_{DD}=3.5V\sim 5.5V$ -40°C < Ta < 85°C*
		13.92*	16*	18.08*		$V_{DD}=4.75V\sim 5.5V$ -40°C < Ta < 105°C*
$V_{ADC}$	Workable ADC operating Voltage	2.5		5.0	V	
$V_{AD}$	AD Input Voltage	0		$V_{DD}$	V	
$V_{DR}$	RAM data retention voltage*	1.5			V	In power-down mode.

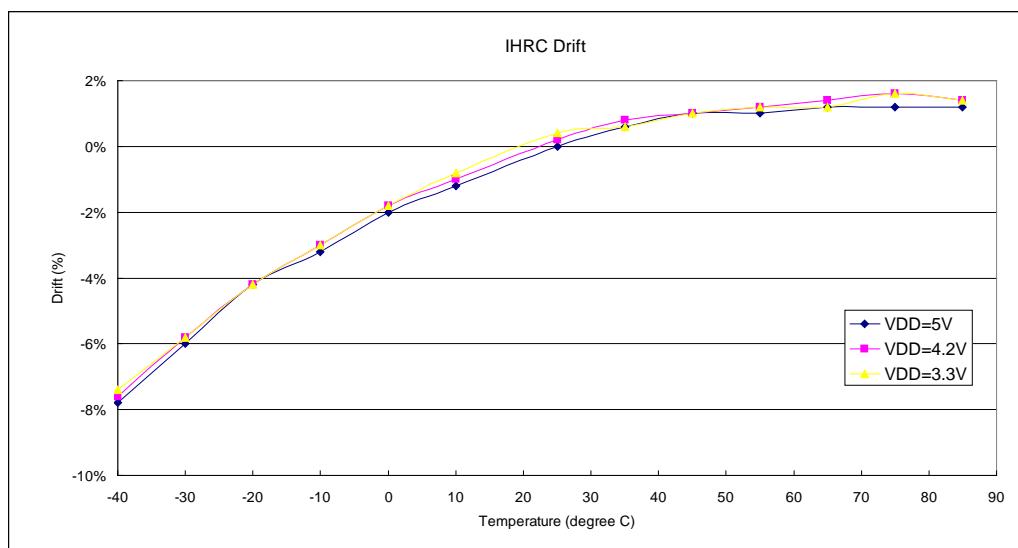
\*These parameters are for design reference, not tested for each chip.

The larger  $f_{IHRC}$  drift will have adverse effect on the RPM accuracy for DF329 DC Fan application.

### 3.2. Absolute Maximum Ratings

- Supply Voltage ..... 2.2V ~ 5.5V
- Input Voltage ..... -0.3V ~  $V_{DD}$  + 0.3V
- Operating Temperature ..... -40°C ~ 105°C
- Junction Temperature ..... 150°C
- Storage Temperature ..... -50°C ~ 125°C

### 3.3. Typical IHRC frequency deviation vs. VDD and temperature (calibrated to 16MHz)



### 3.4. Typical Operating Current vs. VDD and CLK=IHRC/n

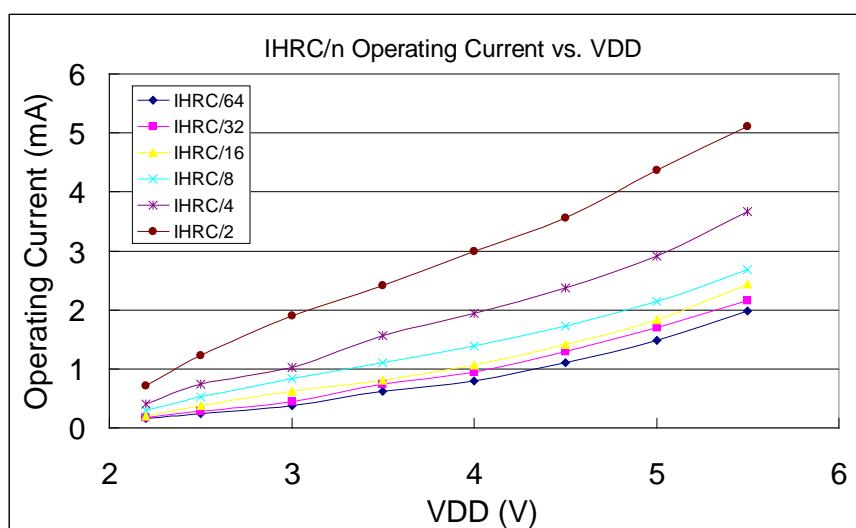
Conditions:

1-FPPA (code option)

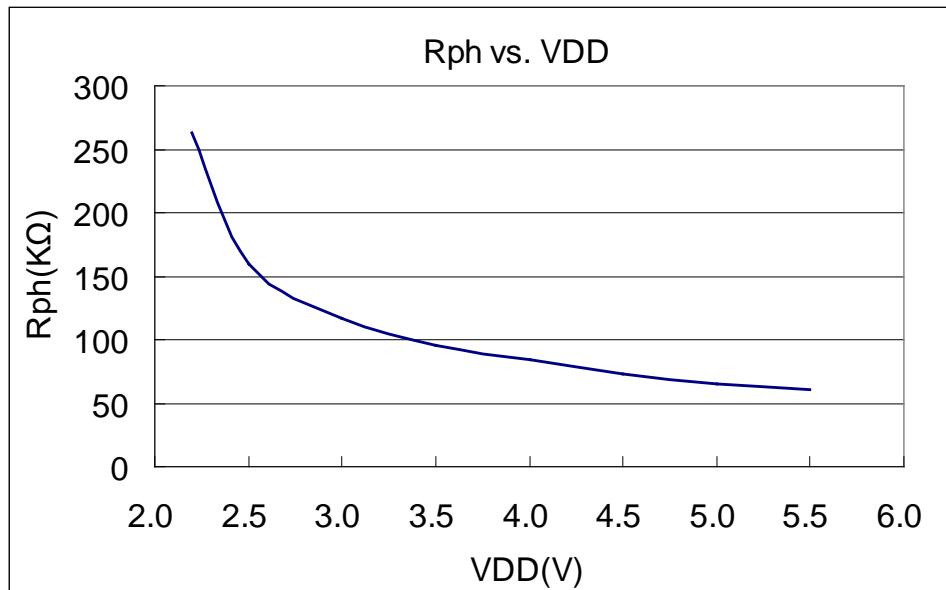
**ON**: Band-gap, LVD, IHRC;

**OFF**: ILRC, EOSC, T16, TM2, ADC, PWM, Hall Comparator modules;

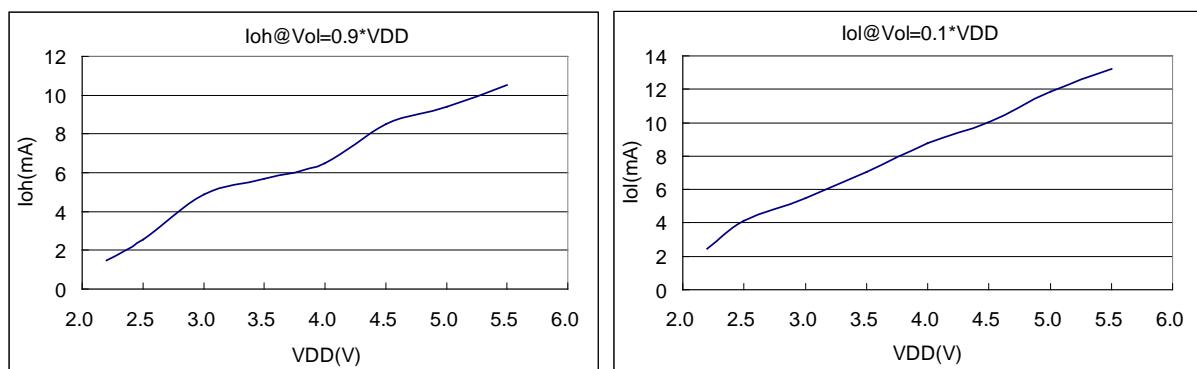
**IO**: PA0:0.5Hz output toggle and no loading, others: input and no floating



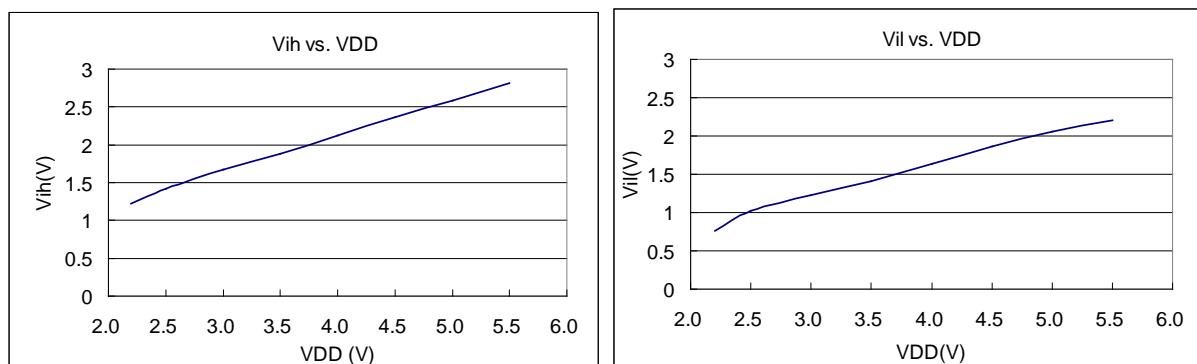
### 3.5. Typical IO pull high resistance



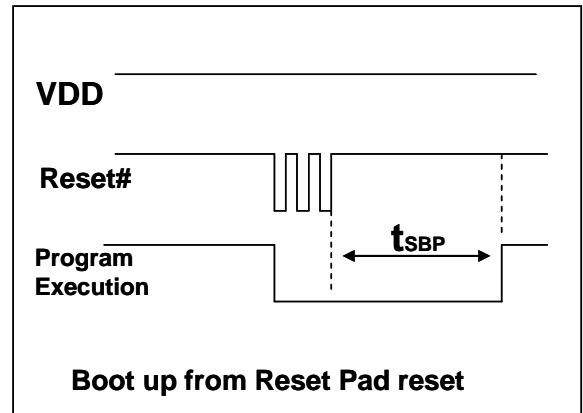
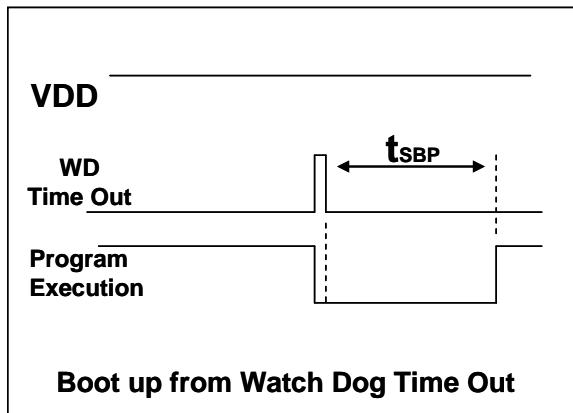
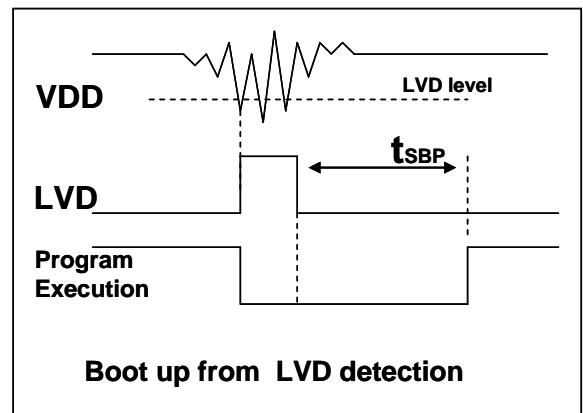
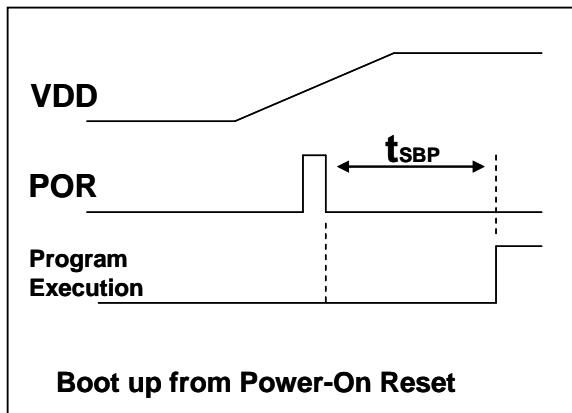
### 3.6. Typical IO driving current (I<sub>OH</sub>) and sink current (I<sub>OL</sub>)



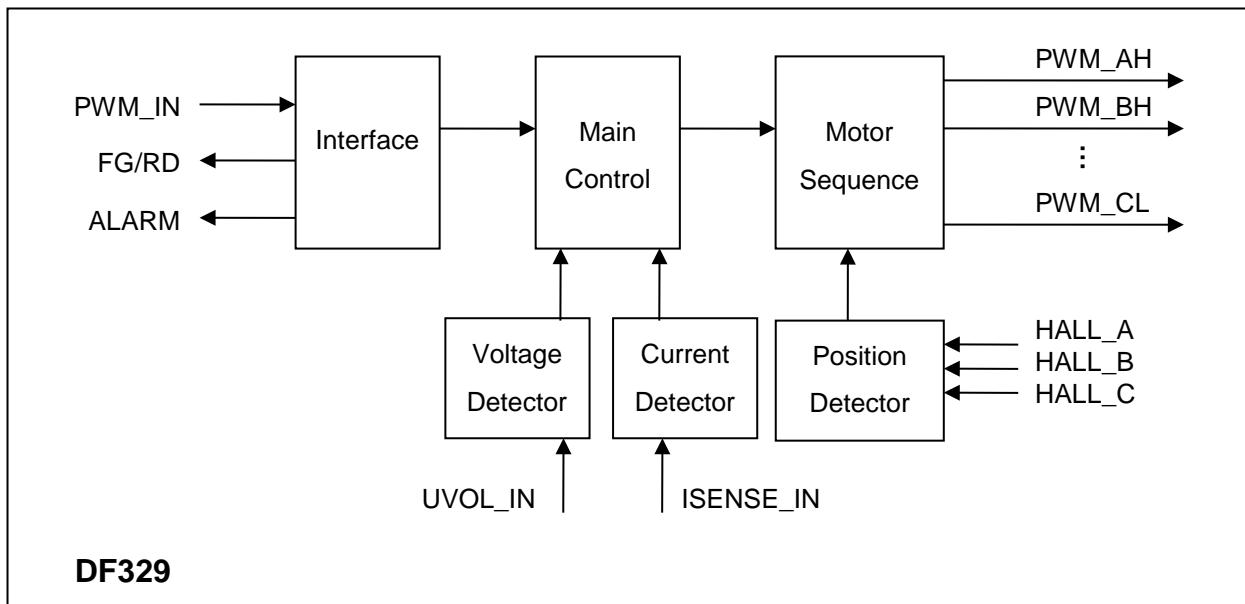
### 3.7. Typical IO input high/low threshold voltage (V<sub>IH</sub>/V<sub>IL</sub>)



### 3.8. Timing charts for boot up conditions



### 4. Block Diagram



### 5. Functional Description

DF329 is a controller which is target for 3-phase brushless DC motor with hall sensor; there are five functional modules inside the DF329: Main Control, Current Detector, Motor Sequence Control, Position Detector and Interface. Its functional descriptions are shown as below:

#### 5.1. Main Control

This Main Control module is coordinator to maintain the finite state of the system. It receives the command passed by user interface detector and motor current from current detector module, and then determines the next action for motor based on those two received conditions.

#### 5.2. Current Detector

This module is used to detect the feedback current of motor (**ISENSE\_IN**) and send to main control module, the main control will stop the motor and set alarm output whenever the sensing current reaches the value corresponding to over current protection.

#### 5.3. Voltage Detector

This module is used to detect the feedback voltage of motor (**UVOL\_IN**) and send to main control module, the main control will stop the motor and set alarm output whenever the sensing voltage reaches the value corresponding to under voltage over low protection.

### 5.4. Motor Sequence Control

The motor sequence control module controls the power MOSFET ON/OFF of motor. It depends on the position information sent by position detector module to output the six driving signals (PWM\_AH, PWM\_AL, PWM\_BH, PWM\_BL, PWM\_CH, and PWM\_CL) that can be directly associated to the sequence phase of motor.

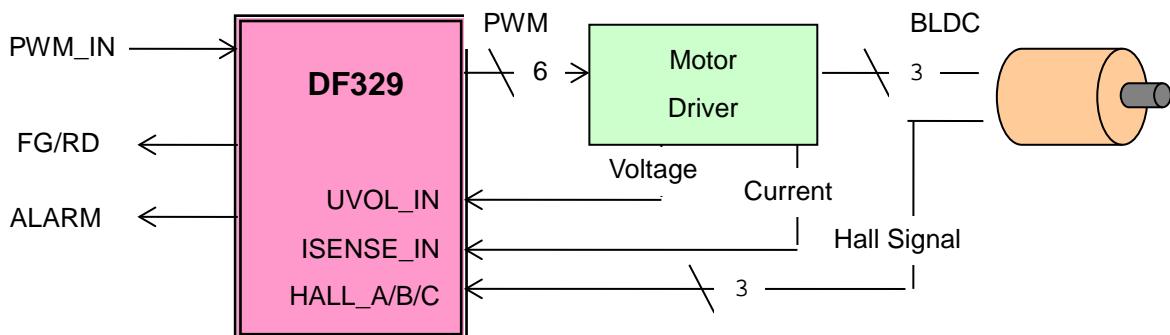
### 5.5. Position Detector

This module is used to detect the feedback hall signals of motor (HALL\_A, HALL\_B, and HALL\_C) and send to motor sequence control module, the sequence control module will decide the next sequence phase to drive the motor.

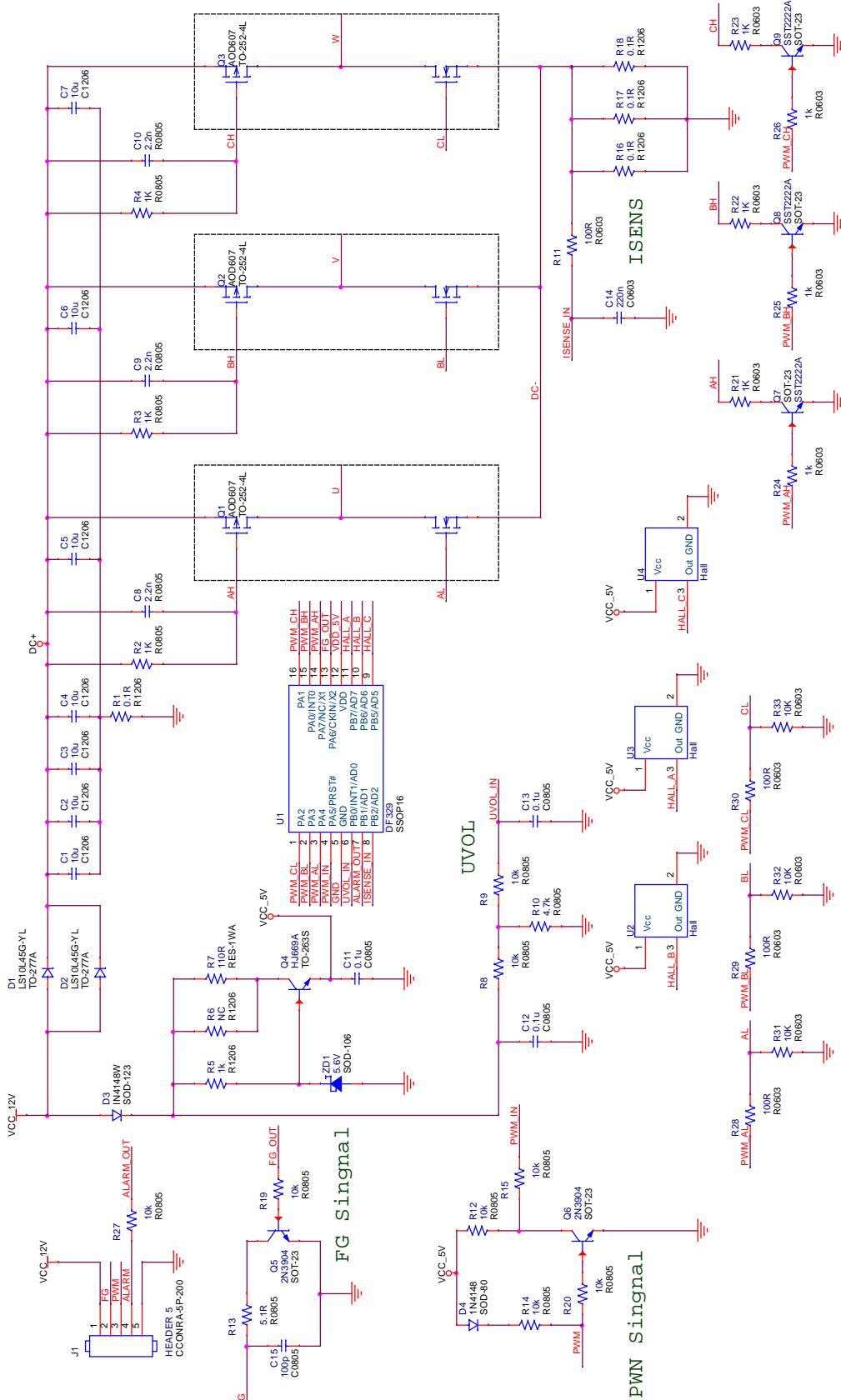
### 5.6. Interface

This module is used to detect the user interface, including PWM input, FG output and ALARM output.

## 6. Application Diagram



### 6.1. Reference Application Circuit



## 7. Package Marking Information

### 7.1. Marking Information

SSOP16

Example: blank

Example: code

PPP PPPP PPPPPP CCCC CCCC CCCC SSSS SSSSSS SSSSSSSS yy yyww yywwV yywwVXA
---

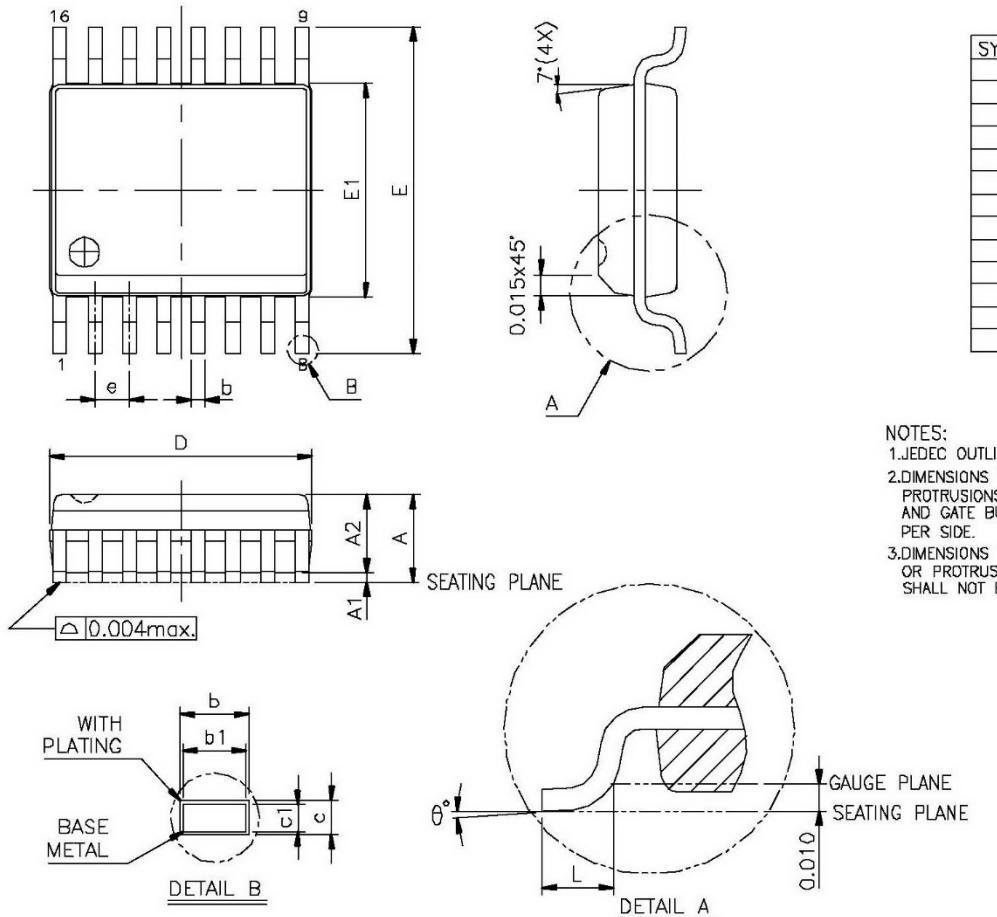
DF329PDFF HJ02351 1848ABK
---------------------------------

DF329A001 HQ12345 1850ABK
---------------------------------

#### Project Legend

PPP PPPP	Product name (Ex: DF329 )
CCCC	Customer's production code number (If blank that CCCC will be PDFF.)
yy	Year code (last 2 digits of calendar year)
ww	Week code
V	Vender code
X	Serial number
A	Wafer information

### 7.2. SSOP16 IC Drawing



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	—	0.059
b	0.008	0.012
b1	0.008	0.011
c	0.007	0.010
c1	0.007	0.009
D	0.189	0.197
E1	0.150	0.157
E	0.228	0.244
L	0.016	0.050
e	0.025	BASIC
θ°	0	8

UNIT : INCH

#### NOTES:

- 1.JEDEC OUTLINE : MO-137 AB
- 2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
- 3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

### 8. POR for DC Fan Application

As shown in Fig 8-1, DF329 generates a good power on reset (POR) signal when VDD rises from 0V to 5V in  $T_{POR}$  (max. 50ms) and rises through the voltage range of 0.7V to 1.6V in  $T_{FSV}$  (max. 10ms).

If there are a lot of abnormal power noises in VDD power-on time period and  $T_{POR}$  and  $T_{FSV}$  do not meet the specifications, DF329 is not able to guarantee circuit initialization and may cause a malfunction.

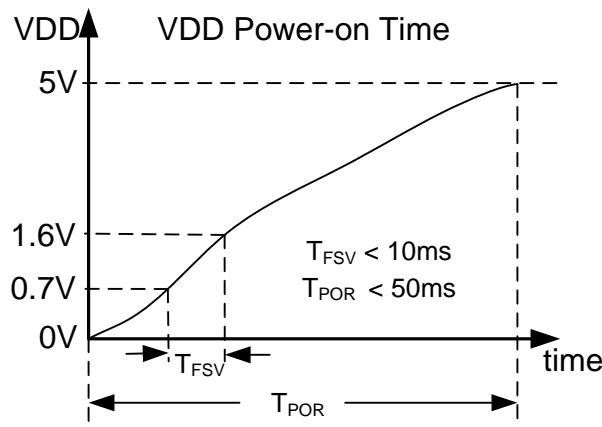


Fig. 8-1

During power-off as shown in Fig 8-2 and Fig 8-3, VDD has to be discharged to  $V_{PDRV}$  (max. is 0.7V) for the next power-on. In case VDD is more than  $V_{PDRV}$ , it is not recognized to do the next power-on.

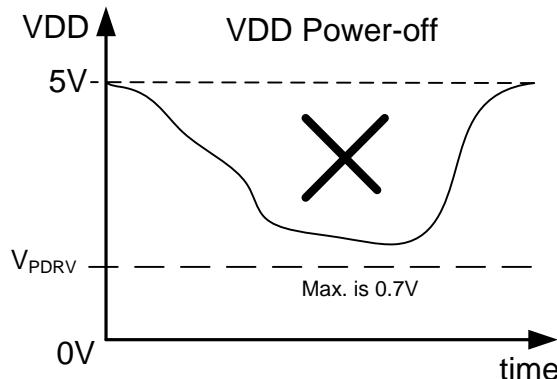


Fig. 8-2

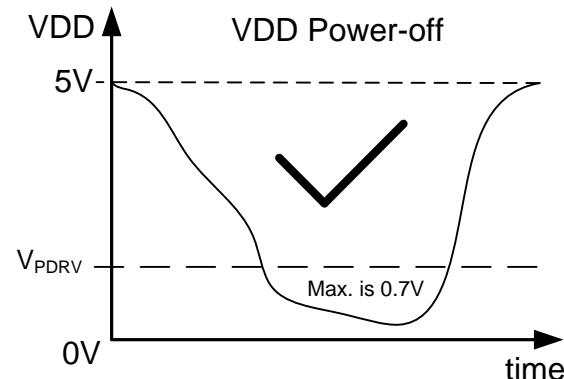


Fig. 8-3

#### **NOTICE:**

**It may cause DF329 malfunction, fail or crash when power-on and power-off do not meet the specifications.**  
**Another proper POR is needed in order to get rid of such status.**

### 9. Programming the DF329

For using the writer (P-002) to program the code, please put the jumper on the CN40.

